REMARKS

This Application has been carefully reviewed in light of the Office Action mailed August 17, 2009. At the time of the Office Action, Claims 1-20 were pending in this Application. Claims 1-20 were rejected. Claims 1 and 20 are herein amended. Applicants respectfully request reconsideration and favorable action in this case.

Amended Independent Claims 1 and 20 are Allowable.

Claims 1-4, 6-8, 10-11 and 20 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Application Publication No. 2002/0040420 ("*Yamauchi*") in view of U.S. Patent Application Publication No. 2003/0084336 ("*Anderson*").

In order to establish a prima facie case of obviousness, the references cited by the Examiner must disclose all claimed limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). Even if each limitation is disclosed in a combination of references, however, a claim composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. *KSR Int'l. Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1741 (2007). Rather, the Examiner must identify an apparent reason to combine the known elements in the fashion claimed. *Id.* "Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Id.*, citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006). Finally, the reason must be free of the distortion caused by hindsight bias and may not rely on ex post reasoning. *KSR*, 127 S.Ct. at 1742. In addition, evidence that such a combination was uniquely challenging or difficult tends to show that a claim was not obvious. *Leapfrog Enterprises, Inc. v. Fisher-Price, Inc. and Mattel, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007), citing *KSR*, 127 S.Ct. at 1741.

Applicants submit that *Yamauchi* and *Anderson*, whether considered alone or in combination, do not teach all limitations of Applicants' claims. For example, amended independent Claims 1 and 20 recite "***the state of a protective layer on the integrated circuit is monitored such that when a breach of the protective layer is detected, data is automatically deleted from at least one memory of the integrated circuit.***"

Neither *Yamauchi* nor *Anderson* teach these limitations In addition, none of the other reference cited by the Examiner teach these limitations, in particular *Anthony* (U.S. Patent Publication No. 2003/0206388), which the Examiner cited as teaching Claim 13's limitation regarding details of the protective layer.

Yamauchi. The Examiner acknowledges that *Yamauchi* does not teach monitoring the state of a protective layer on an integrated circuit (Office Action, bottom page 3).

Anderson. The Examiner alleges that paragraphs 0008 and 0014 of *Anderson* teaches monitoring the state of a protective layer on an integrated circuit. (Office Action, page 4). Applicants respectfully disagree. Paragraph 0008 teaches:

> [0008] Our invention is adapted from dual-rail encoded asynchronous logic because in this technology, the power consumed can be made substantially independent of the data being processed, and by the choice of suitable design rules, which should be clear to those skilled in the art, the design can be made resistant to single-transistor and single-wire faults. Furthermore, such circuits are already known to be highly resilient to variations in the applied power supply voltage. In our invention, alarms resulting from environmental sensors or from the activation of other protective mechanisms can be propagated rapidly through the chip using many independent paths.

Applicants assume the Examiner is referring specifically to the passage teaches "alarms resulting from environmental sensors or from the activation of other protective mechanisms can be propagated rapidly through the chip using many independent paths." However, the passage merely teaches activation of protective mechanisms in general, but does not disclose the specific protective mechanism recited in Applicants' amended claims -- namely, ***monitoring a protective layer*** on the integrated circuit. Further, the passage certainly does not teach *automatically deleting data* from memory on the integrated circuit when a breach of a protective layer is detected.

Paragraph 0014 of *Anderson* teaches:

> [0014] A processor pipeline with a quad-coded data-path may be constructed using well known dual-rail pipelining techniques [3]. Alarm signals can be inserted using an OR function of the data and with a sense signal from a sensor (see FIG. 1). One sensor in our invention is based on an instruction counter; the processor software can check that the expected

> number of instructions have been executed and alarm if this is riot [sic] the case (as might happen, for example, under destructive probing attack). In the single circuit implementing the instruction by which this alarm is executed, we depart from the quad-coded logic rules described herein so that an alarm hardware state may be generated from a non-alarm hardware state. Other sensors are outside the scope of this patent but may typically be designed to detect out-of-bounds environmental parameters such as over- and under-voltage and low temperature. This OR function can be combined with the combinational function indicated to assist the usual gate minimisation process.

Like paragraph 0008 discussed above, paragraph 0014 does not teach anything about a ***protective layer*** on the integrated circuit, much less *automatically deleting data* from memory on the integrated circuit when a breach of a protective layer is detected.

Anthony. The Examiner alleges that paragraphs 0101 and 0151 of *Anthony* teach the various details of the protective layer recited in Applicants' Claim 13. However, *Anthony* is not directed to encryption or data security, but rather to shielding a device against electric charges. Thus, the "protective layer" taught by *Anthony* is actually a conductive shield to protect an electrical component. Accordingly, *Anthony* does not teach monitoring for a breach of the "protective layer," much less *deleting data* from memory when a breach of the "protective layer" is detected. Thus, *Anthony* clearly does not teach the limitations of amended Claims 1 and 20.

For at least the reasons discussed above, amended independent Claims 1 and 20 are allowable over the cited references. Therefore, Applicants respectfully request allowance of Claims 1 and 20, as well as all claims that depend from Claim 1.

Dependent Claims 5, 9, 12, 13, and 14 are Allowable.

Dependent Claims 5, 9, 12, 13, and 14 were rejected under 35 U.S.C. §103(a) as being unpatentable over various combination of *Yamaichi*, *Anderson*, *Nakajima* (U.S. Patent Publication No. 2004/0106239, *Fricke* (U.S. Patent No. 6,711,045), *Khoury* (U.S. Patent Publication No. 2001/0053565), *Anthony* (U.S. Patent Publication No. 2003/0206388), *Huttunen* (U.S. Patent Publication No. 2003/0147267), and *Kean* (U.S. Patent Publication No. 2001/0015919.

Applicants submit that dependent Claims 5, 9, 12, 13, and 14 are allowable at least because they depend from independent Claim 1, shown above to be allowable. Accordingly, Applicants respectfully request allowance of dependent Claims 5, 9, 12, 13, and 14. Applicants do not concede that any of the proposed combinations are proper.

CONCLUSION

Applicants have made an earnest effort to place this case in condition for allowance in light of the remarks set forth above. Applicants respectfully request reconsideration of the pending claims.

Applicants believe there are no fees due at this time. However, the Commissioner is hereby authorized to charge any fees necessary or credit any overpayment to Deposit Account No. 50-4871 of King & Spalding L.L.P.

If there are any matters concerning this Application that may be cleared up in a telephone conversation, please contact Applicants' attorney at 512-457-2030.

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